Christian Lanius

PHD CANDIDATE IN ELECTRICAL ENGINEERING

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Objective

Research low power, efficient digital designs in advanced technologies, exploiting regularity. Automating tooling and flows to explore the design space and make the research reproducible.

Experience

RWTH Aachen | PhD Candidate **2020 – Today**

- Develop a cadence tool based digital implementation with automatic design space exploration
- Design of a template based synthesis and implementation flow for regular designs
- Design of an accelerated platform on FPGA for genome alignment with HLS and RTL
- 3x Tapeout in 22nm FDSOI: Tapeout lead, chip level design, RTL2GDS flow implementation
- Specification of PCBs and probecard as test platform and bring-up/silicon validation
- Guide bachelor and master students during labs, classes and as thesis supervisor

Rohde & Schwarz | Intern **2017**

- Use of System Generator for DSP (Simulink) to implement receiver for GBAS signaling
- Validation on hardware with signal generator and visualization/post-processing in MATLAB

RWTH Aachen University | Student Assistant **2015 – 2019**

- FPGA based pre-processing platform for ultrasonic sensor data
- Evaluation of open-source autonomous driving platform

Education

RWTH Aachen University, Germany | M.Sc. Electrical Engineering **2016 – 2019**

Major: Micro- and Nanoelectronics | Grade: 1.0 (GPA: 4.0)

Keio University, Japan | M.Sc. Engineering **2017 – 2019**

Major: Integrated Design Engineering | GPA: 3.94

RWTH Aachen University, Germany | B.Sc. Electrical Engineering **2013 – 2016**

Major: Micro- and Nanoelectronics | Grade: 2.1 (GPA: 2.9)

Skills & Abilities

- Cadence tools for digital implementation: Genus, Innovus, Quantus, Voltus, Conforml
- Xilinx tools: Vivado, Vitis, Petalinux, XRT
- Siemens/Mentor tools: Questasim, Calibre (DRC, LVS)
- GF Technologies: 22nm FDSOI, 12nm LP+
- Languages: Systemverilog, Python, TCL, c

Publications

First Author

- C. Lanius and T. Gemmeke, "Fully Digital, Standard-Cell-Based Multifunction Compute-in-Memory Arrays for Genome Sequencing," in IEEE TVLSI, vol. 32, no. 1, pp. 30-41, Jan. 2024, doi: 10.1109/TVLSI.2023.3308262
- C. Lanius, J. Lou, J. Loh and T. Gemmeke, "Automatic Generation of Structured Macros Using Standard Cells – Application to CIM," 2023 IEEE/ACM ISLPED, Vienna, Austria, 2023, doi: 10.1109/ISLPED58423.2023.10244608
- C. Lanius, F. Freye, S. Zhang and T. Gemmeke, "Hardware Trojans in fdSOI," 2023 IEEE/ACM ISLPED, Vienna, Austria, 2023, doi: 10.1109/ISLPED58423.2023.10244573
- C. Lanius and T. Gemmeke, "Multi-Function CIM Array for Genome Alignment Applications built with Fully Digital Flow," 2022 IEEE NorCAS, Oslo, Norway, 2022, doi: 10.1109/NorCAS57515.2022.9934470 (Best paper award candidate)
- C. Lanius, D. Kobayashi, K. Ouchi and Y. Aoki, "Single Image, Context Aware Action Estimation in Sports," 2018 SITIS, Las Palmas de Gran Canaria, Spain, 2018, pp. 664-671, doi: 10.1109/SITIS.2018.00107
- C. Lanius, D. Hedderich, S. Mohammed, G. Ascheid and V. Lücken, “Deep-Learning Based Depth Completion for Autonomous Driving Applications,” Smart Transportation, pp. 183-213, doi: 10.1201/9780367808150-9

Co-Author (Excerpt)

- J. Lou, C. Lanius, F. Freye, T. Stadtmann and T. Gemmeke, "All-Digital Time-Domain Compute-in-Memory Engine for Binary Neural Networks With 1.05 POPS/W Energy Efficiency," 2022 IEEE ESSCIRC, Milan, Italy, 2022, pp. 149-152, doi: 10.1109/ESSCIRC55480.2022.9911382
- V. Lücken, N. Voss, J. Schreier, T. Baag, M. Gehring, M. Raschen, C. Lanius, R. Leupers and G. Ascheid, “Density-Based Statistical Clustering: Enabling Sidefire Ultrasonic Traffic Sensing in Smart Cities,” Journal of Advanced Transportation. 2018. 10.1155/2018/9317291
- J. Lou, F. Freye, C. Lanius and T. Gemmeke, "Scalable Time-Domain Compute-in-Memory BNN Engine with 2.06 POPS/W Energy Efficiency for Edge-AI Devices”, 2023 ACM GLSVLSI, Knoxville, USA, 2023, pp. 665-670, doi: 10.1145/3583781.3590220
- J. Lou, F. Freye, C. Lanius and T. Gemmeke, "An Energy Efficient All-Digital Time-Domain Compute-in-Memory Macro Optimized for Binary Neural Networks," in TCAS I: Regular Papers, vol. 71, no. 1, pp. 287-298, Jan. 2024, doi: 10.1109/TCSI.2023.3323205
- D. Fallnich, C. Lanius, S. Zhang, and T. Gemmeke, “Efficient ASIC Architecture for Low Latency Classic McEliece Decoding”, TCHES, vol. 2024, no. 2, pp. 403–425, 2024, doi: 10.46586/tches.v2024.i2.403-425
- K. Kauth, C. Lanius and T. Gemmeke, “nAIxt: A Light-Weight Processor Architecture for Efficient Computation of Neuron Models,” ARCS 2024. Lecture Notes in Computer Science, vol 14842. Springer, Cham. doi:10.1007/978-3-031-66146-4_1